| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/790,516 | TALWALKAR ET AL. | |
| | Examiner | Art Unit | |
| | Lana N. Le | 2618 | |

*-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/01/04*.

2. ☒ The allowed claim(s) is/are *1-23*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## *REASON FOR ALLOWANCE*

1. Claims 1-23 are allowable over the cited prior art.

2. The following is an examiner's statement of reasons for allowance:

Regarding independent claim 1, Narumi et al (US 6,118,811) disclose a method for controlling transmit signals, the method comprising:

calibrating in a transmitter (22) having an analog step amplifier (30; fig. 1) by detecting the transmitter output and generating calibrating signals via a DSP (50) to measure the transmitter output and correcting the analog transmitter gain output and then coupling the known calibration signal levels into to a receiver mixer (150) to adjust and calibrate a receiver (24) (col 5, line 60 – col 6, line 32).

Holoubek et al (US 5,590,418) disclose a method for stabilizing a gain of a control loop by adjusting a digital stepped attenuator (302) when the transmitter output power is ramped below its maximum level during a time period between bursts (col 4, lines 54-65).

Narumi et al, Holoubek et al, and the cited prior art fail to disclose:

calibrating an analog step attenuator by applying a digital attenuator to determine an accuracy in attenuation of the analog step attenuator; and using the determined accuracy of the analog step attenuator to facilitate realization of a predetermined attenuation using both the analog step attenuator and the digital attenuator.

Regarding independent claim 12, Holoubek et al disclose a method for achieving a change in attenuation, the method comprising:

applying smaller increments of attenuation to a digital attenuator (302) (col 5, lines 16-20);

comparing a resulting change in attenuation (gain change) to a predetermined attenuation threshold (stored optimum gain stabilization value in processor 308); and

changing attenuation (via correction signal 309) of the digital attenuator according to the predetermined attenuation threshold (col 4, line 54 - col 5, line 28). Holoubek et al and the cited prior art fail to disclose the method comprising:

applying smaller increments of attenuation to a digital attenuator relative to known increments of attenuation capable in an analog step attenuator;

changing attenuation of an analog step attenuator and the digital attenuator according to the predetermined attenuation threshold.

Regarding independent claim 18, Narumi et al disclose a digital signal processor (50 and 52; fig. 1) comprising:

a signal generation unit (130) to output a digital modulated signal (col 5, lines 2-5);

a digital tuner (132) coupled to the signal generation unit (130), the digital tuner (132) configured to provide a digital signal with a selected frequency rate to a digital-to-analog converter (52) and an analog step attenuator (30) outside the digital signal processor (50);

an open loop calibration control block (154, 150, 56, 58) configured to receive a signal output from a baseband filter (58), the baseband filter (58) configured to receive the analog signal output (154) from the analog step attenuator (30) (col 5, lines 17-43).

However, Narumi et al and the cited prior art fail to disclose the digital signal processor comprising:

the signal generation unit coupled to an input multiplexer to receive the digital modulated signal;

a digital attenuator coupled to the input multiplexer, the digital attenuator configured to provide an attenuated signal to the digital-to-analog converter;

a closed loop calibration control block;

a storage block configured to receive control signals from the closed loop calibration control block, the storage block providing a calibrated step size indicative of an accuracy in attenuation of the analog step attenuator; and

an open loop ramp up/down control block coupled to the storage block to apply the determined accuracy of the analog step attenuator to facilitate realization of a predetermined desired attenuation using both the analog step attenuator and the digital attenuator.

Regarding independent claim 22, Narumi et al disclose an integrated circuit (fig. 1) comprising:

a signal generation unit (130) coupled to output a digital modulated signal (col 5, lines 2-5);

a digital tuner (132) coupled to the signal generation unit (130), the digital tuner (132) configured to provide an digital signal with a selected frequency rate to a digital-to-analog converter (52) and an analog step attenuator (30) outside the digital signal processor (50, 52);

an open loop calibration control block (154, 150, 56, 58) configured to receive a signal output from a baseband filter (58), the baseband filter (58) configured to receive the analog signal output (154) from the analog step attenuator (30) (col 5, lines 17-43). However, Narumi et al and the cited prior art fail to disclose the integrated circuit comprising: the signal generation unit coupled to an input multiplexer, a storage block configured to receive control signals from a closed loop calibration control block,

a digital attenuator coupled to the input multiplexer, the digital attenuator configured to provide an attenuated signal to the digital-to-analog converter;

a storage block providing a calibrated step size indicative of an accuracy in attenuation of the analog step attenuator;

an open loop ramp up/down control block coupled to the storage block to apply the determined accuracy of the analog step attenuator to facilitate realization of a predetermined desired attenuation using both the analog step attenuator and the digital attenuator.

Regarding independent claim 23, Holoubek et al a system for attenuating a signal, the system comprising:

a plurality of operating components (212, 214, 302, 308, 306, 304, 224, 226, 228) including at least a digital attenuator (302) and an analog step attenuator (212),

the operating components (212, 214, 302, 308, 306, 304, 224, 226, 228) operable during a normal mode, the operating components configured to apply smaller increments of attenuation (via correction signal 309) to the digital attenuator (302) (col 5, lines 16-20), the operating components configured to change attenuation of the

analog step attenuator (via 202 from feedback loop) and the digital attenuator (302) according to a predetermined attenuation threshold (stored in processor 308) (col 4, line 54 - col 5, line 28).

Holoubek et al and the cited prior art fail to disclose the system comprising:

a plurality of calibration components; the plurality of operating components coupled to the calibration components, the operating components including one or more of the calibration components;

the applying of the attenuation to the digital attenuator is relative to known increments of attenuation capable in the analog step attenuator, one or more of the operating components configured to compare a resulting change in attenuation to a predetermined attenuation threshold determined by one or more of the calibration components.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## ***Conclusion***

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Skarby (US 6,334,050), Arrangement and a Method Relating to a Radio Unit

- Huang et al (US 6,885,241), Type Based Baseband Predistorter Function Estimation Technique for Non-linear Circuits

- Baker et al (US 6,606,483), Dual Open and Closed Loop Linear Transmitter.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N. Le whose telephone number is (571) 272-7891. The examiner can normally be reached on M-F 9:30-18:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lana N. Le
5-28-06

Lana Le

LANA LE
PRIMARY EXAMINER